What is claimed is:

1. A pipe latch circuit for storing a plurality of sequentially received first data and second data and outputting them as rising edge output data or falling edge output data, comprising:

a first input register for receiving said first data;

a plurality of first serial pipe latches comprising a plurality of registers connected in series, for selectively storing outputs from said first input register and selectively outputting them;

a first linkage register for storing data outputted from said plurality of first serial pipe latches;

a second input register for receiving said second data;

a plurality of second serial pipe latches comprising a plurality of registers connected in series, for selectively storing outputs from said second input register and selectively outputting them;

a second linkage register for storing data outputted from said plurality of second serial pipe latches;

a multiplexer for selecting data stored in said first linkage register and said second linkage register as rising edge output data or falling edge output data, and outputting them; and

a pipe latch circuit controller for controlling said plurality of first and second serial pipe latches and said multiplexer.

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Abstract of the Disclosure

It is an objective of the present invention to provide a pipe latch circuit with simpler control, smaller footprint, and higher speed operation. For this purpose, the present invention provides a pipe latch circuit for storing a sequentially received plurality of first data and second data and outputting them as rising edge output data or falling edge output data, ~~including: a first input~~ register for receiving the first data; a plurality of first serial pipe latches comprising a plurality of registers connected in series, for selectively storing the outputs from the first input registers and selectively outputting them; a first linkage register for storing the data outputted from the plurality of first serial pipe latches; a second input register for receiving the second data; a plurality of second serial pipe latches comprising a plurality of registers connected in series, for selectively storing the outputs from the second input registers and selectively outputting them; a second linkage register for storing the data outputted from the plurality of second serial pipe latches; a multiplexer for selecting the data stored in the first linkage register and the second linkage register as the rising edge output data and the falling edge output data, and outputting them; and A pipe latch circuit controller for controlling the plurality of first and second serial pipe latches and the multiplexer.

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